

# 1800A/3.3kV IGBT Module using Advanced Trench HiGT

## Structure and Module Design Optimization

Takayuki Kushima, Hitachi Power Semiconductor Device, Ltd., Japan,

[takayuki.kushima.cs@hitachi.com](mailto:takayuki.kushima.cs@hitachi.com)

Katsunori Azuma, Hitachi Power Semiconductor Device, Ltd., Japan,

[katsunori.azuma.em@hitachi.com](mailto:katsunori.azuma.em@hitachi.com)

Yasuhiro Nemoto, Hitachi Power Semiconductor Device, Ltd., Japan,

[yasuhiro.nemoto.jw@hitachi.com](mailto:yasuhiro.nemoto.jw@hitachi.com)

Katsuaki Saito, Hitachi Europe Ltd., United Kingdom,

[katsuaki.saito@hitachi-eu.com](mailto:katsuaki.saito@hitachi-eu.com)

Yoshihiko Koike, Hitachi Power Semiconductor Device, Ltd., Japan,

[yoshihiko.koike.zp@hitachi.com](mailto:yoshihiko.koike.zp@hitachi.com)

### Abstract

1800A/3.3kV IGBT module with the highest current rating was developed. Advanced Trench HiGT structure was used to achieve low loss characteristics. Module electrical and thermal characteristic were optimized in order to reduce thermal resistance and parasitic inductance. The current ratings of new IGBT module can be increased by 20% from the conventional product type.

### 1. Introduction

The 3.3kV IGBT modules are being used widely in the traction [1], medium and high voltage converters [2] with the configuration of 2-level, 3-level and multiple unit configurations. In such a versatile applications, one of the standard package sizes is 140mm x 190mm x 38mm (Fig.1), and the highest current rating in the accessible market is 1500A. IGBT modules having high output with compatible package size are needed to exploit design resources and to reduce development cost.

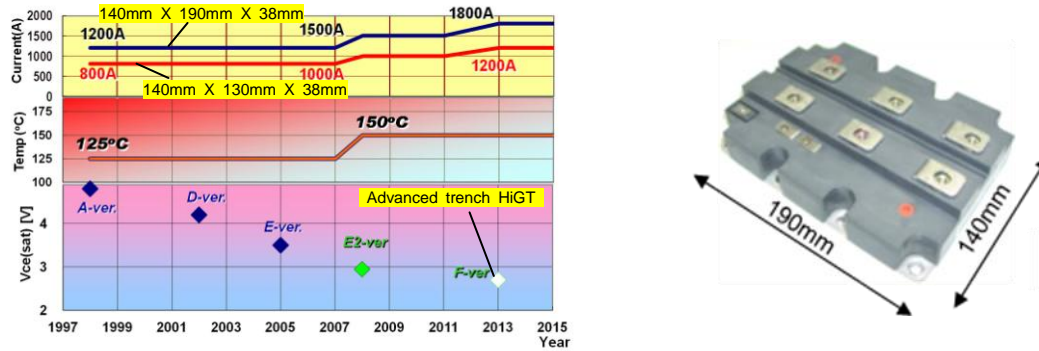
To meet the needs from application side, we developed the new IGBT module with higher current rating. In order to realize the challenging target, it is essential not only to adopt low loss characteristics of Si chip design, but also to optimize and improve the thermal, mechanical, and electrical aspect of packaging. We have already shown the low loss characteristics of Si chip design without sacrificing gate controllability [3][4][5].

In this paper, we demonstrate the optimization of thermal and electrical design of the packaging.

### 2. Target of the Development, and Design Concept

Fig.1 shows the Hitachi 3.3kV IGBT module trend with regard to current rating, junction temperature, and typical  $V_{ce(sat)}$ . At the conventional product type, maximum current rating is 1500A and 1000A for 140mm x 190mm x 38mm and 140mm x 130mm x 38mm respectively.

In this development, we aimed to increase the rated current by 20% from conventional maximum 1500A and achieve the rated current 1800A. Fig.2 shows the target specification implemented.



**Fig. 1.** Hitachi's 3.3kV IGBT trend(Left) and external appearance of 140mm X 190mm size IGBT module(Right)

## 2.1. Target of thermal design

First, thermal point of view is due to the following.

$$\Delta T_j = P \cdot R_{th}(j - ambient) = Const. \quad (1)$$

where,

$$R_{th}(j - ambient) = R_{th}(j - c) + R_{th}(c - hs) + R_{th}(hs - ambient) \quad (2)$$

In case of replacing conventional product, it is not expected to reduce the  $R_{th}(c-hs)$  and  $R_{th}(hs-ambient)$ . Therefore, we set the  $R_{th}(j-c)$  target more than 20% reduction, and loss P target more than 20% reduction. Concept of target setting is as follows.

Switching loss is proportional to the  $I_C$  in the first approximation. For this reason, switching loss will increase 20% when  $I_C$  is increased by 20%. Further, it is a rule of thumb, the conduction loss is proportional to 3/2 power of the  $I_C$ . For this reason, the conduction loss will increase 30% when  $I_C$  is increased by 20%. Thus,  $R_{th}(j-ambient)$  is desired to reduce 20-30%, if possible. However even 20% lower  $R_{th}(j-c)$ , reducing the  $R_{th}(j-ambient)$  is about 10% at most. Therefore we have decided to reduce 20% loss(P) to suppress  $\Delta T_j$ .

In addition, terminal resistance target is set more than 44% reduction to maintain a constant terminal temperature.

## 2.2. Target of electrical design

### Stray inductance reduction

Electrical point of view is due to the following. In order to suppress the surge voltage as equivalent to conventional,

$$\Delta V_{CE} = L_s \cdot \frac{dI_C}{dt} = Const. \quad (3)$$

where,

$$L_s = 2 \cdot L_s(\text{IGBT}) + L_s(\text{Busbar}) + L_s(\text{Capacitor}) \quad (4)$$

In a system optimized  $L_s(\text{Busbar})$  and  $L_s(\text{Capacitor})$ , each inductance values are nearly the same. And in case of replacing conventional, it is not expected to reduce the  $L_s(\text{Busbar})$  and  $L_s(\text{Capacitor})$ . Therefore, we set the  $L_s(\text{IGBT})$  target more than 40% reduction.

### Gate driving compatibility

It is also important to consider gate driving compatibility in order to replace conventional products.

Gate driver circuit power loss  $P_G$  can be calculated from an examination of the gate electric charge characteristics, and is represented by the following equation [6].

$$P_G = \{ |V_{GP}| + |V_{GN}| \} \cdot Q_G \cdot f_C \quad (5)$$

Therefore, we set  $Q_G$  target equivalent or less than that of conventional products.

### Electrical durability

Electrical durability required for IGBT is RBSOA(Reverse Bias Safe Operating Area), RRSOA(Reverse Recovery Safe Operating Area), SCSOA(Short Circuit Safe Operating Area) and surge current capability. Surge current capability is represented by  $I^2t$  value in the datasheet.

In order to increase rated current 20%, we set each target as follows, RBSOA and RRSOA; more than 20% increase, SCSOA; same,  $I^2t$  value; more than 44% increase at  $T_j=150^\circ\text{C}$ .

## 2.3. Other packaging design

Package size is same as conventional products from the view of compatibility.

No.	Item		Target	Action
1	Current rating(A)		+20%	-
2	Packaging size		Equivalent	-
3	Thermal Design	Thermal resistance(Rth(j-c))	<-20%	• Chip rearrangement (Including chip size)
4		Loss(P)	<-20%	• Chip upgrade (Advanced Trench HiGT)
5		Terminal resistance	<-44%	• Terminal design (Electrical resistance reduction) • Ultrasonic Welding (Terminal - Substrate)
6	Electrical Design	Stray Inductance	-40%	• Terminal design (Closely Spaced Terminals)
7		Vg-Qg characteristics	Equivalent	• Chip upgrade (Advanced Trench HiGT)
8	Durability	RBSOA	+20%	• Chip upgrade (Advanced Trench HiGT) • Stray inductance reduction • Imbalance suppression of internal inductance
9		RecSOA	+20%	• Stray inductance reduction • Expansion of active size • Imbalance suppression of internal inductance
10		SCSOA	Equivalent	• Chip upgrade (Advanced Trench HiGT) • Imbalance suppression of internal inductance
11		$I^2t$	>+44%	• Reduction of conduction loss • Reduction of thermal resistance

Fig. 2. Subject for Development

### 3. Thermal and Electrical Optimization of the Packaging Design

#### 3.1. Improvement of loss reduction using 3.3kV advanced trench HiGT

The new IGBT adopted the advanced trench gate structure (Advanced Trench HiGT structure [4][5]) with deep floating-p layer to realize the improvement of  $V_{ce(sat)}$  vs.  $E_{off}$  trade-off relationship. The thickness of n-type bulk layer and structure of backside are tuned and optimized for soft switching and reduction of  $V_{ce}$  spike at turn off. The advanced trench HiGT structure is shown in Fig.3 by comparison with conventional IGBT. The characteristic structures are the floating p-layer separated from the trench gates. This gate structure can suppress excess  $V_{GE}$  overshoot at IGBT turn-on and at the same time,  $I_{rp}$  of diode recovery decrease.

The improvement of  $V_{CE(sat)}$  vs.  $E_{off}$  trade-off relationship and  $V_F$  vs.  $E_{on+Err}$  trade-off relationship of new IGBT module are shown in Fig. 4.

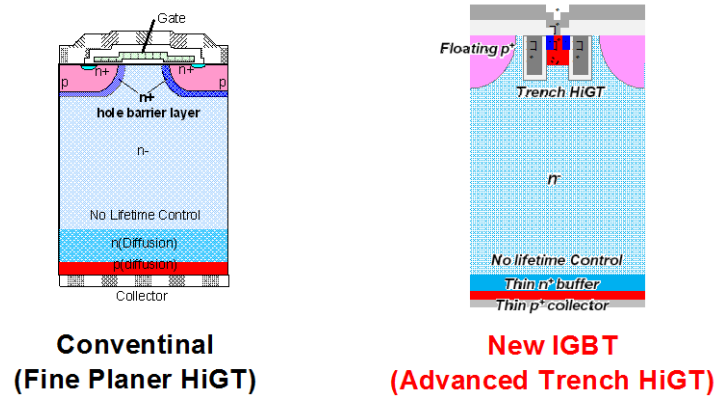


Fig. 3. IGBT unit cell structure

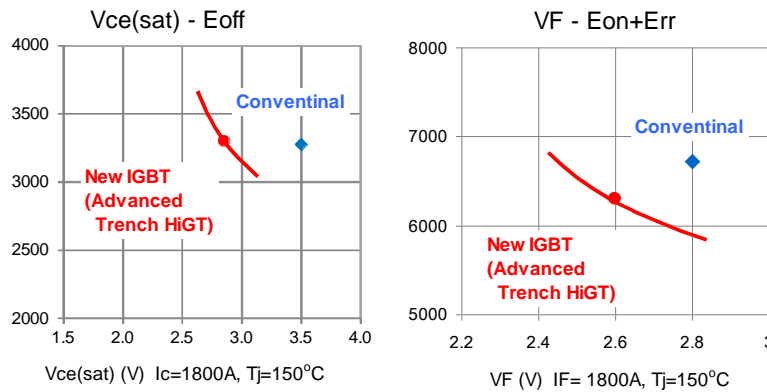


Fig. 4. Trade-off – comparison with conventional product type

#### 3.2. Chip rearrangement for thermal and electrical optimization

In order to optimize thermal resistance, chip layout is rearranged. Areas of diodes are enlarged and dispersed in order to the effective heat spread. Enlarging areas of diodes is also for achieving surge current durability [7]. 3 layout patterns are evaluated to reduce imbalance of junction temperature and parasitic inductance. Advantages and disadvantages of each layout is following (Fig.5).

- 1) A straight arrangement
- 2) A staggered arrangement
- 3) A pseudo-staggered arrangement

A straight arrangement is the best in terms of electrical because of ease of aligning the wire length, but the hot spot is generated by thermal interference. On the other hand, a staggered arrangement is the best in terms of thermal because of suppression of thermal interference, but it is difficult to suppress imbalance of parasitic inductance and reduce it by asymmetric structure. As a compromise, a pseudo-staggered arrangement is chosen.

Fig.6 shows comparison of the imbalance of parasitic inductance and current imbalance. Current sharing of a pseudo-staggered arrangement is same level as conventional product type.

As a result, thermal resistance 20% reduction is achieved without compromising electrical characteristics.

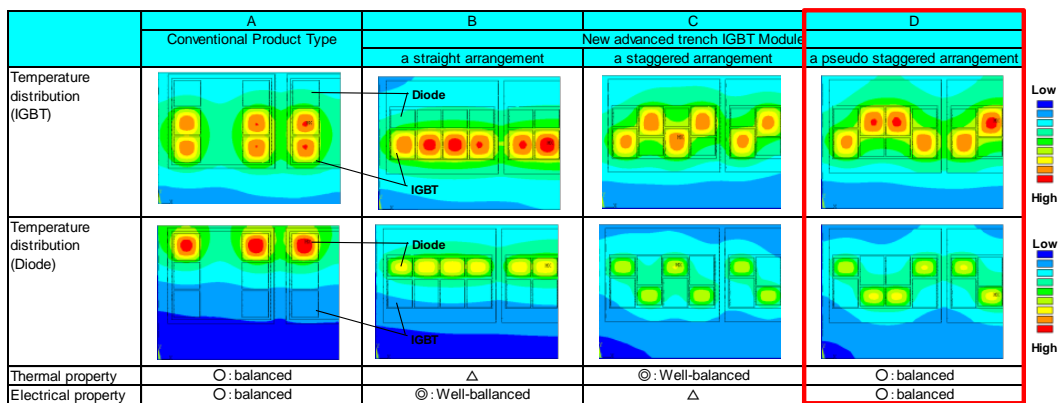


Fig. 5. Comparison of temperature distribution

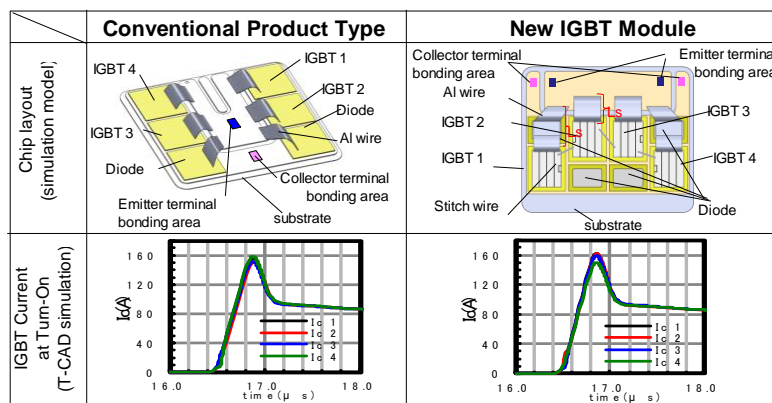


Fig. 6. Comparison of the imbalance of parasitic inductance and current imbalance(simulation)

### 3.3. Terminal Design to minimize the stray inductance and resistance

Terminal structures are optimized to reduce the stray inductance and resistance. Fig. 7 shows comparison of the main terminal structure [8]. Emitter terminal and a collector terminal of new IGBT are disposed close to each other like a parallel plate. In addition, sectional area of terminal is increased and length of terminal is reduced in order to minimize its resistance.

Terminal connection between the substrates is applied ultrasonic welding process in order to ensure the reliability of a large current flowing. Stress relieving structure is provided for reducing stress on the terminal – substrate junction part due to stress in the thermal cycle. Further, imbalance of the inductance is adjusted to suppress current imbalance between the substrates.

As a result, 45% reduction of terminal resistance and 40% reduction of stray inductance are achieved. Terminal current is able to be increased 15% from conventional products at same terminal temperature rise (Fig.8).

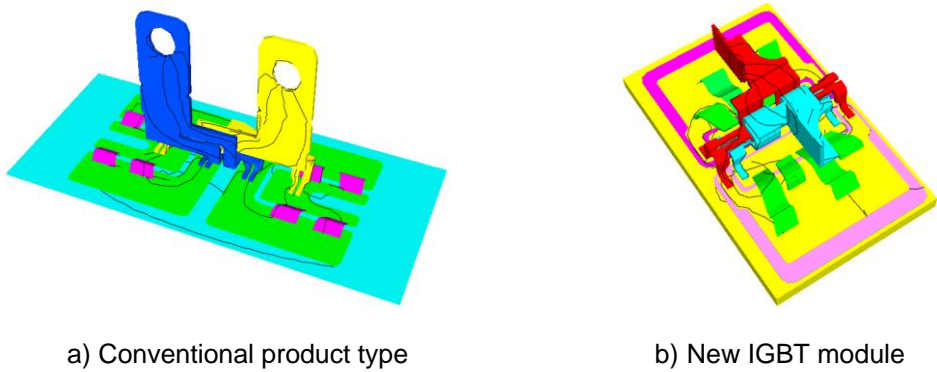
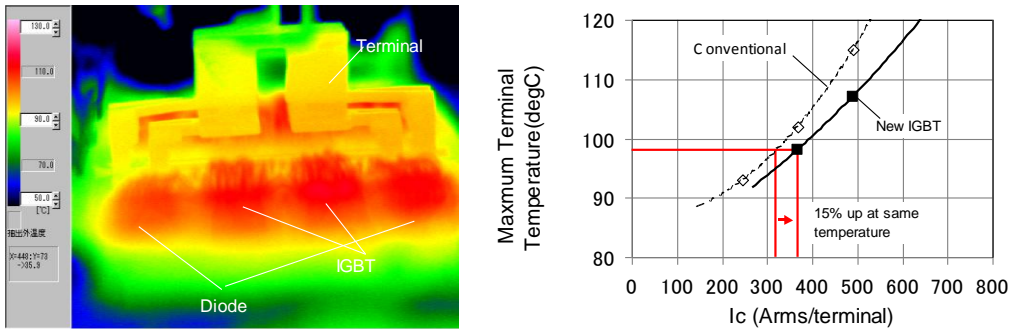


Fig. 7. Comparison of the main terminal structure (Stray inductance simulation)



a)Thermoviewer image of terminal temperature b)comparison of the terminal temperature

Fig. 8. Mesurament result of terminal temperature of the new IGBT module

### 4. Electrical Characteristics

#### 4.1. Gate electric charge characteristics

Gate charge characteristic of new IGBT is equivalent to conventional (Fig.9). Therefore, new IGBT can be easily replaced to conventional one.

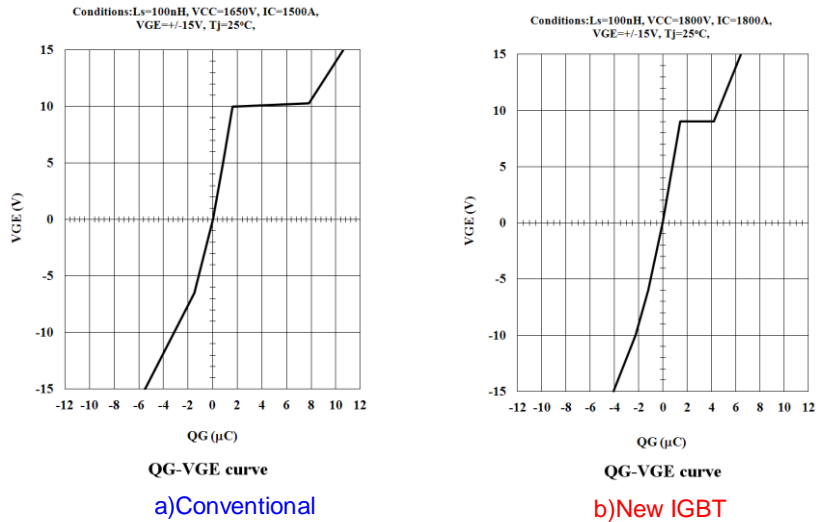


Fig. 9. Gate electric charge characteristics

#### 4.2. Electrical durability

Fig.10 shows the waveform of RBSOA and RRSOA. And Fig.11 shows the waveform of SCSOA and  $I^2t$  value. From the result of this, target specifications of electrical durability are achieved.

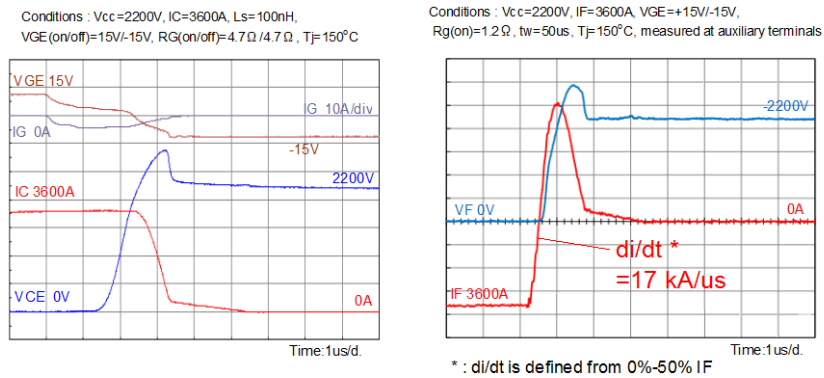


Fig. 10. RBSOA(Left) and RRSOA(Right)

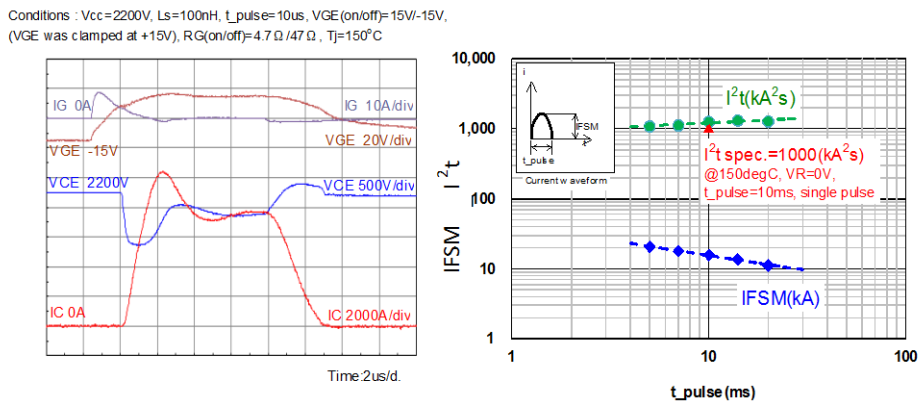


Fig. 11. SCSOA(Left) and Surge current capability(Right)

### 4.3. Maximum phase current

Maximum phase current is calculated and is shown in Fig.12. By achieving the target specifications in Fig.2, 20% improvement in output current is achieved.

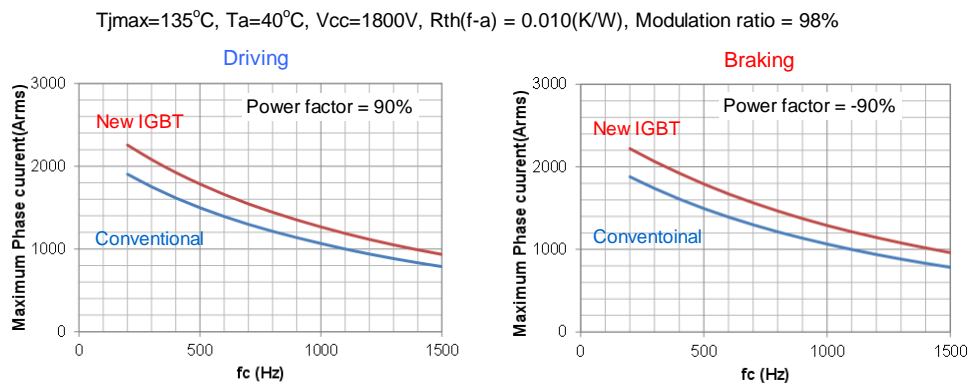


Fig. 12. Calculation of maximum phase current

## 5. Conclusion

We develop the 1800A/3.3kV IGBT module with the highest current rating which is 20% increase from conventional. Its target is able to replace conventional product without changing heatsinks, capacitors, busbars, and gate drivers. 20% increase of output current is achieved.

## 6. Reference

- [1] A. Nagel, M. Bakran, "Robustness Requirements on Semiconductors for High Power Applications", Proc. 15<sup>th</sup> EPE, 2013
- [2] P.S. Jones, C.C. Davidson, "Calculation of Power Losses for MMC-based VSC HVDC Station", Proc. 15<sup>th</sup> EPE, 2013
- [3] M. Mori, K. Oyama, Y. Kohno, J. Sakano, J. Uruno, K. Ishizaka, D. Kawase, "A Trench-Gate High-Conductivity IGBT (HiGT) With Short-Circuit Capability", IEEE Transact. on Elec. Dev, vol.54, No.8, pp.2011-2016, Aug. 2007,
- [4] T. Arai, S. Watanabe, K. Ishibashi, Y. Toyoda, T. Oda, K. Saito, M. Mori, "The Advanced Trench HiGT with Separate Floating p-Layer for Easy Controllability and Robustness", Proc. PCIM Europe 2011, pp.329-335, 2011
- [5] Y. Toyota, M. Wakagi, K. Ishibashi, H. Mizue, Y. Shima, T. Oda, D. Kawase, K. Saito and M. Mori, "Novel 3.3-kV Advanced Trench HiGT with Low Loss and Low dv/dt Noise", Proc. 25<sup>th</sup> ISPSD., pp.29-36, 2013
- [6] Hitachi Power Semiconductor Device, Ltd., Application Manual for High voltage IGBT module, <http://www.hitachi-power-semiconductor-device.co.jp/en/product/igbt/attention.html>, 2009
- [7] J. Lutz, H. Shlangenotto, U. Scheuermann, R. De Doncker, "Semiconductor Power Devices. Physics, Characteristics, Reliability", Springer, pp.421-426, 2011.
- [8] K. Azuma, I. Yoshida, A. Konno, Y. Toyoda, K. Saito, "New 3.3kV IGBT Module with Low Power Loss and High Current Rating," Proc. PCIM Europe 2013, pp.345-350., 2013